***Semester: 4th (Regular&Back)(Back)***

**Sub & Code: CS - 2006**

**Branch (s): CSE & IT**

**kiitlogo SPRING END SEMESTER EXAMINATION-2017**

**COMPUTER ORGANIZATION AND ARCHITECTURE**

**[CS-2006]**

**Full Marks: 60 Time: 3 Hours**

***Answer any six questions including question No.1 which is compulsory.***

***The figures in the margin indicate full marks.***

***Candidates are required to give their answers in their own words as far as practicable and***

***all parts of a question should be answered at one place only.***

Q No: Contents Marks

1. Short Questions [2 × 10]
2. Consider a computer that has a byte-addressable memory organized in 32-bit words according to the big-endian scheme. A program reads ASCII characters entered at a keyboard and stores them in successive byte locations, starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the name "Johnson" has been entered.
3. Consider a processor with 64 registers and an instruction op-code of size twelve bits. Each instruction has five distinct fields namely op-code, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, then how much amount of memory (in bytes) consumed by the program?
4. Show how to implement a full adder by using two half adders and external logic gates, as necessary.
5. Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB. How many number of bits in the TAG, SET and WORD fields, respectively?
6. Difference between memory mapped I/O and I/O mapped I/O
7. How cycle-stealing mode is different from burst mode data transfer in DMA.
8. A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds. 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively. When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?
9. State and explain the cache coherence problem and its solution.
10. A main memory unit with a capacity of 4 megabytes is built using 1M x 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. What will be the time required to perform one refresh operation on all the cells in the memory unit?
11. Consider the following scenario: We want to read 1024 bytes in programmed I/O mode CPU. The bus width is 32 bits, each time an interrupt occurs from hard disk and it takes 3 micro seconds to service it. How much CPU time is required to read 1024 bytes?
12. [2 × 4]
13. A two word instruction LOAD is stored at location 300 with its address field in the next location. The address field has the value 600 and the value stored at 600 is 500 and at 500 is 650. The words stored at 900, 901, and 902 are 400, 401 and 402 respectively. A processor register *R* contains the number 800 and index register has value 100. Evaluate the effective address and operand if addressing mode of the instruction is as follows:
14. Immediate
15. Indirect
16. Relative
17. Index
18. Write the micro routine for the following instruction. Assume second operand is also the destination register.
19. ADD 50(R1), R2
20. SUB R3, (R4)+
21. [2 × 4]
22. Draw and explain 3-bus CPU organization and write the control signals to execute following instruction using same organization. Assume second operand is also the destination register.

ADD (R1)+, R2

1. Let a cache with 8 words block; a read miss occur so for that entire block is to be loaded. Find the time required to access the block for memory without interleaved and with interleaved (4 modules), if the hardware properties are:
2. It takes 1 clock cycle to send address to main memory.
3. First word of block will be transferred by 8 clock cycles and other words will take 4 clock cycles using fast page mode.
4. 1 clock cycle is needed to send one word to the cache memory.
5. [2 × 4]
6. Design of 16-bit carry-lookahead adder build from 4-bit adders.
7. Multiplication of two numbers 45 × 63 by using carry-save addition process.
8. [2 × 4]
9. Assume you want to organize a nested subroutine calls on a computer as follows: the routine Main calls a subroutine SUB1 by executing a two-word call subroutine instruction located in memory at address 1000 followed by the address field of 6000 at location 1001. Again subroutine SUB1 calls another subroutine SUB2 by executing a two-word call subroutine instruction located in memory at address 6050 followed by the address field of 8000 at location 6051 . The content of the top of the memory stack is 5000. The content of the stack pointer SP is 3000. What are the content of PC, SP, and the top of the stack?
   * + 1. After the subroutine call instruction is executed in the main routine?
       2. After the subroutine call instruction is executed in the subroutine SUB1?
       3. After the return from SUB2 subroutine?
       4. After the return from SUB1 subroutine?
10. Explain the importance of interrupt vector in I/O Processing? What is daisy chain method for handling simultaneous interrupt request.
11. [2 × 4]
12. Divide 12 ÷ 5 using restoring and non-restoring division algorithm.
13. What is parallel processing? Discuss Flynn's classification with suitable diagram.
14. [2 × 4]
15. Multiply two numbers (-25) × (-16) using Booth's algorithm. Give the flow table of multiplication.
16. Write the IEEE 754 format for representing floating point numbers in double precision format. Represent the decimal number -10.125 using IEEE 754 double precision floating point format. What is the value of E' and mantissa M to represent the special values 0, ∞. NaN, and denormal numbers in this representation?
17. Write Short Notes ( Answer Any Two) [2 × 4]
18. Von-neuman architecture Vs Havard architecture
19. Hardwired Control Unit Vs Microprogrammed Control Unit
20. RISC Vs CISC
21. Memory mapped I/O Vs I/O mapped I/O

Paper Setter: Himansu Das

Moderator……………………….

Controller of Examinations